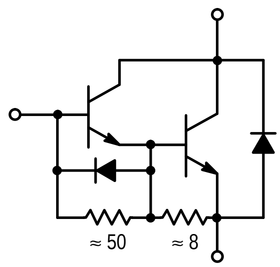
MJ10015
MJ10016

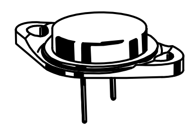
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 AND 500 VOLTS
250 WATTS

The MJ10015 and MJ10016 Darlington transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  1.0 µs (max) Inductive Crossover Time — 20 Amps
  2.5 µs (max) inductive Storage Time — 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
  Reversed Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents





CASE 197–05
TO–204AE TYPE
(TO–3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector–Emitter Voltage	V_{CEO}	400	500	Vdc
Collector–Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75		Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10015		$V_{CEO(sus)}$	400	—	—	Vdc
MJ10016			500	—	—	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	—	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	25	—	—	—
(I_C = 40 Adc, V_{CE} = 5.0 Vdc)			10	—	—	
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	—	—	2.2	Vdc
(I_C = 50 Adc, I_B = 10 Adc)			—	—	5.0	
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	—	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	—	—	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 µs Duty Cycle ≤ 2%).	t_d	—	0.14	0.3	µs
Rise Time		t_r	—	0.3	1.0	µs
Storage Time		t_s	—	0.8	2.5	µs
Fall Time		t_f	—	0.3	1.0	µs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	—	1.0	2.5	µs
Crossover Time		t_c	—	0.36	1.0	µs

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.
(2) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads.
Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

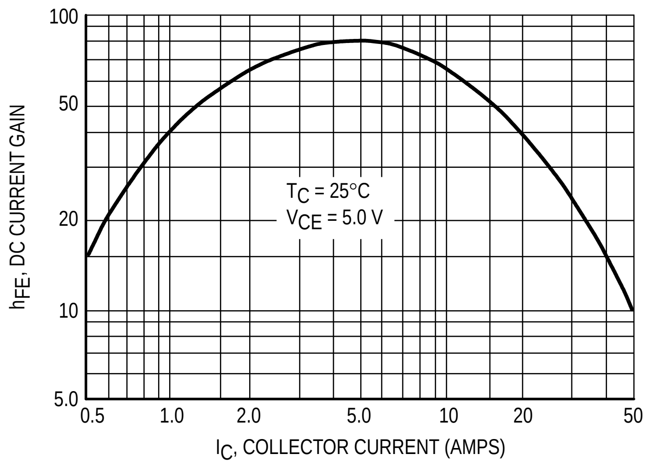


Figure 1. DC Current Gain

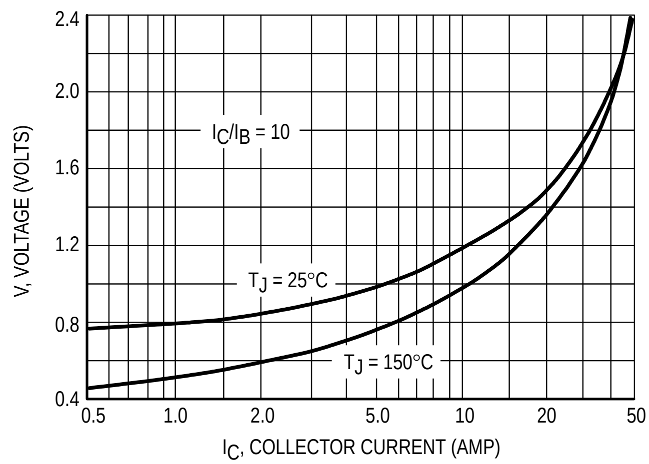


Figure 2. Collector–Emitter Saturation Voltage

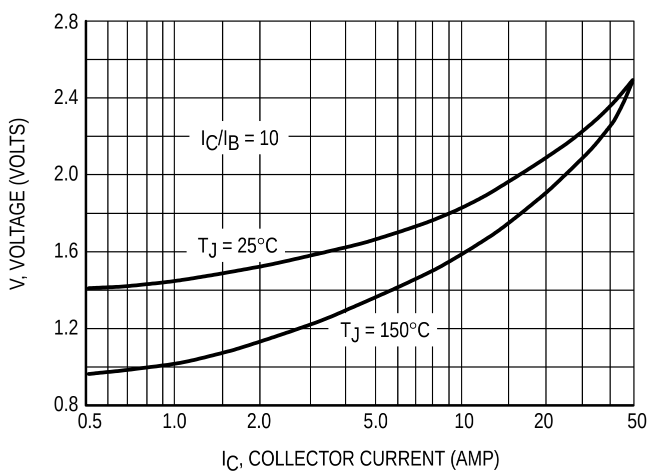


Figure 3. Base–Emitter Saturation Voltage

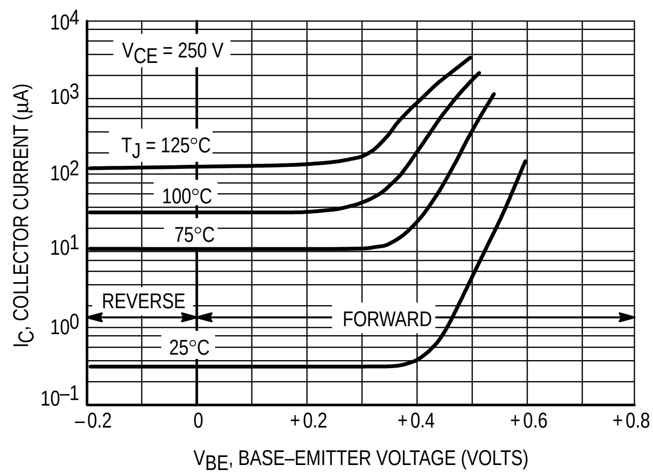


Figure 4. Collector Cutoff Region

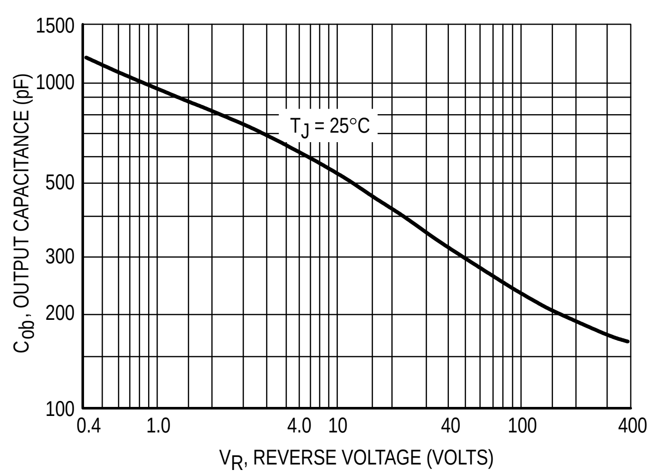
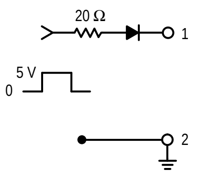
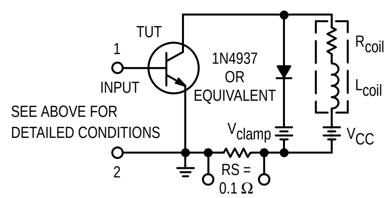
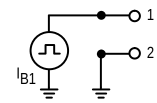
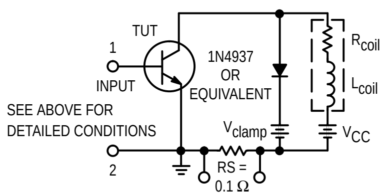
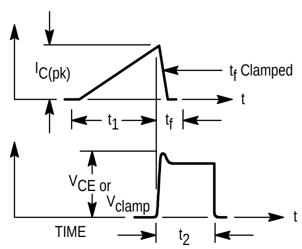
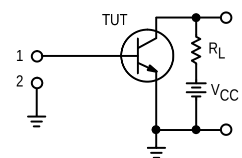


Figure 5. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	V_{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	INDUCTIVE TEST CIRCUIT 	TURN–ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

* Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 8).

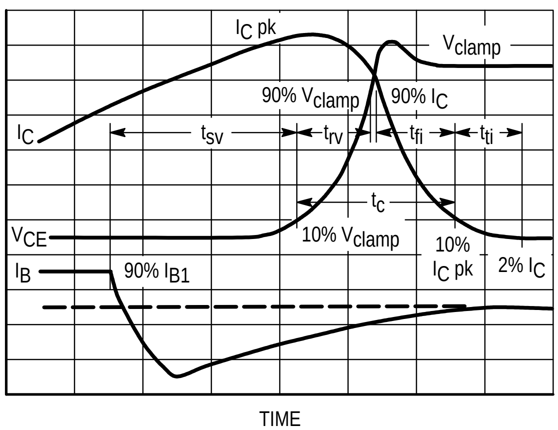


Figure 6. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

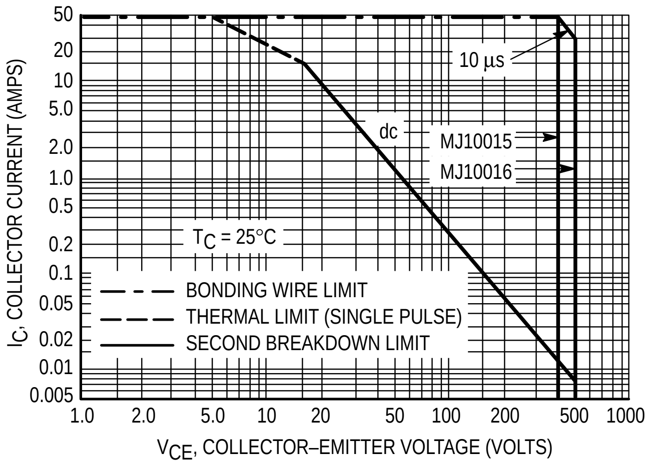


Figure 7. Forward Bias Safe Operating Area

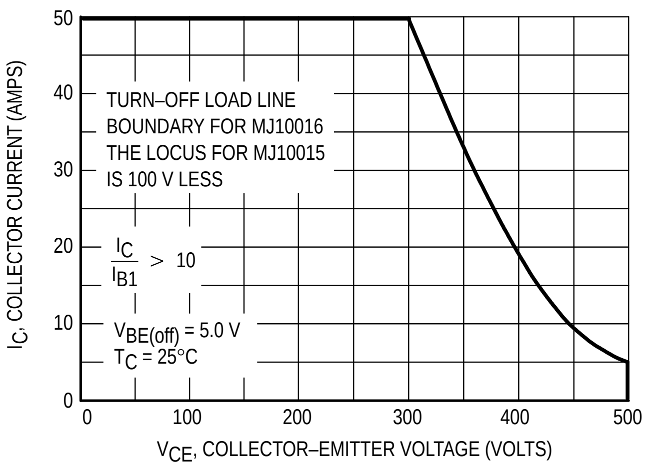


Figure 8. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

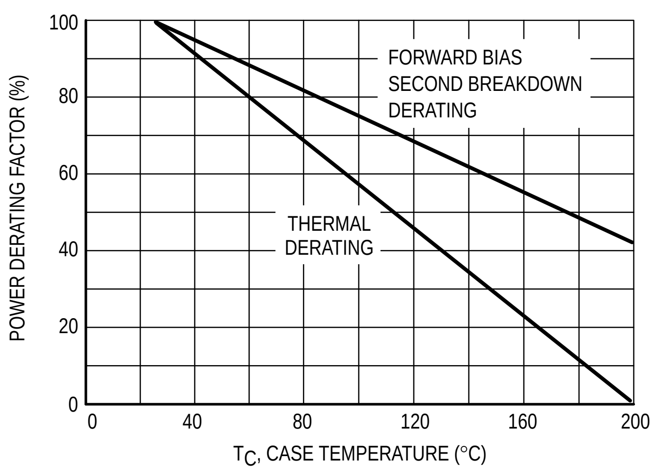


Figure 9. Power Derating

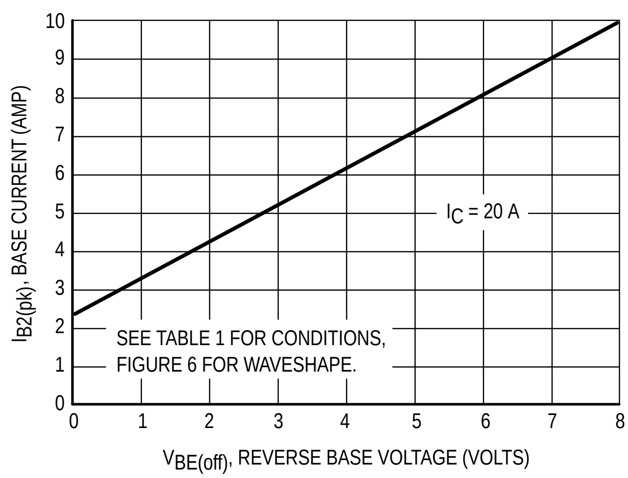
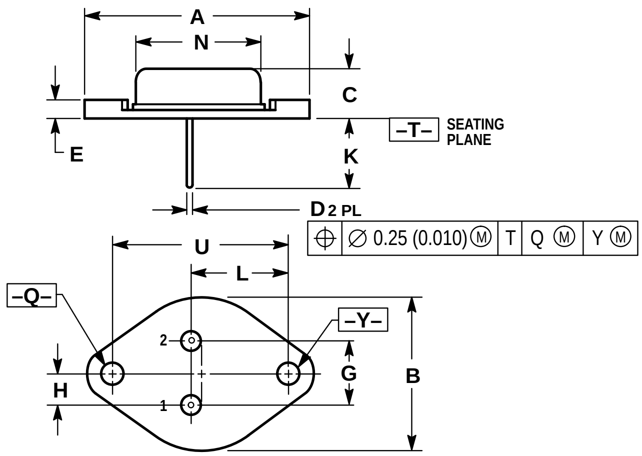


Figure 10. Typical Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	0.980	1.050	24.89	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.135	1.52	3.43
G	0.420	0.440	10.67	11.18
H	0.205	0.225	5.21	5.72
K	0.440	0.480	11.18	12.19
L	0.655	0.675	16.64	17.15
N	0.760	0.830	19.30	21.08
Q	0.151	0.175	3.84	4.19
U	1.177	1.197	29.90	30.40

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 197–05
TO–204AE TYPE
(TO–3 TYPE)
ISSUE J

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